Problem 2.14

Determine the closed-loop gain of the circuit shown below, assuming an ideal op amp. All of the resistors are equal in value.

Solution: Let's number the resistors and their corresponding currents from left to right in the feedback loop of this circuit. The summing point constraint requires that the voltage at the (-) and (+) inputs are both 0.

The current through the input resistor is \( i_{in} = \frac{V_{in}-0}{R} \) (from left to right).

Since no current goes into or out of the (-) input, we will have \( i_1 = i_{in} \) (both are left to right).

To be consistent, I have chosen direction of the "horizontal" currents as left-to-right (\( \rightarrow \)) and the "vertical" currents as upward (\( \uparrow \)).

Kirchhoff's Current Law applied to the two junctions gives \( i_1 + i_2 = i_3 \), and \( i_3 + i_4 = i_5 \).

Kirchhoff's Voltage Law applied to a loop containing resistors 1 and 2 and the (-) and (+) terminals of the op amp gives:
\[ i_1 R - i_2 R + 0 = 0 \implies i_1 = i_2 \]. Then \( i_1 + i_2 = i_3 = 2i_1 \).

Using KVL on the loop containing resistors 2, 3, and 4, gives:
\[ i_2 R + i_3 R - i_4 R = 0 \implies i_2 + i_3 = i_4 = i_1 + 2i_1 = 3i_1 \].

Substituting into \( i_3 + i_4 = i_5 \) gives \( (2i_1) + (3i_1) = 5i_1 = i_5 \).

Finally use KVL on the loop containing resistors 1, 3, 5, \( v_o \), and the (-) and (+) terminals of the op amp.
\[ i_1 R + i_3 R + i_5 R + v_0 + 0 = 0 \implies v_0 = -R[i_1 + 2i_1 + 5i_1] = -8R i_1 \].

If we substitute \( i_{in} = i_1 \), and solve, we get \( A_v = \frac{V_o}{V_{in}} = -8 \).
**Problem 2.15**

The resistors in an inverting amplifier have a tolerance of ±1%. What is the tolerance of the gain?

Solution: The worst cases are \( A_v = \frac{R_f(1+0.01)}{R_i(1-0.01)} = 1.02 \) and \( A_v = \frac{R_f(1-0.01)}{R_i(1+0.01)} = 0.98 \), so the tolerance of ±2%

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**Problem 2.22**

Analyze the ideal op-amp circuit shown below to find an expression for \( v_o \) in terms of \( v_A, v_B \) and the resistor values.

![Circuit Diagram](HW_02b.08.nb)

At the (-) input the voltage is \( V_- = V_o \frac{R_1}{R_1+R_2} \). This must match the voltage at the (+) input because of the summing point constraint.

Using KVL around a loop containing both voltage sources, we find \( V_A - I R_A - I R_B - V_B = 0 \).

Solving for \( I \), gives \( I = \frac{V_A - V_B}{R_A + R_B} \).

Then \( V_+ = V_A - I R_A = V_A - \frac{V_A - V_B}{R_A + R_B} R_A = \frac{V_A R_B - V_B R_A}{R_A + R_B} = V_o \frac{R_1}{R_1+R_2} \).

Solving, \( v_o = \frac{V_A R_B - V_B R_A}{R_A + R_B} \frac{R_1+R_2}{R_1} = \frac{V_A R_B - V_B R_A}{R_A + R_B} \left(1 + \frac{R_2}{R_1}\right) \)

Or \( v_o = A_A v_A - A_B v_B \), where \( A_A = \frac{R_B}{R_A + R_B} \left(1 + \frac{R_2}{R_1}\right) \) and \( A_B = \frac{R_A}{R_A + R_B} \left(1 + \frac{R_2}{R_1}\right) \)
Problems 2.25

For the circuit above:

a) Find an expression for the output voltage in terms of the source current and resistor values.
b) What is the output impedance of this circuit?
c) What is the input impedance of this circuit?
d) This circuit can be classified as an ideal amplifier. What type of amplifier is it?

a) Using KVL: \( i_{in} R_f + V_o = 0 \rightarrow V_o = -i_{in} R_f. \)
b) Because \( V_o \) is independant of \( R_L \), this acts like an ideal voltage source with an output impedance of zero.
c) The input voltage is zero (because of the summing point constraint) \( \rightarrow R_{in} = 0. \)
d) From Table 1.1, we see that this is a transresistance amplifier.

Problems 2.44

A certain op amp has a unity-gain bandwidth of 15 MHz. If this op amp is used in a noninverting amplifier having a dc gain of 10, what is the 3 dB bandwidth? Repeat for a dc gain of 100.

The unity-gain bandwidth, \( f_u \), is 15 MHz. The "closed-loop" gain is \( A_{ocl} = 10. \)

The -3 dB bandwidth is given by: \( f_{bcl} = \frac{f_u}{A_{ocl}} = \frac{15 \text{ MHz}}{10} = 1.5 \text{ MHz}. \)

For \( A_{ocl} = 100 \), we have a -3 dB bandwidth of \( f_{bcl} = \frac{f_u}{A_{ocl}} = \frac{15 \text{ MHz}}{100} = 150 \text{ kHz}. \)

Problems 2.51

Suppose we want to design an amplifier that can produce a 100 kHz sine wave output voltage having a peak output voltage of 5.0 Volts. What is the minimum slew-rate specification for the op amp?

\( f = 100 \text{ kHz (sine wave)} = f_{FP}, \text{ the full-power bandwidth.} \) \( 5.0 \text{ V} = \text{peak voltage} = V_{o\text{max}}. \)

Then, from (2.46), \( f_{FP} = \frac{SR}{2 \pi V_{o\text{max}}}, \rightarrow \text{SR} = (2 \pi V_{o\text{max}}) f_{FP} = 2 \pi (5 \text{ V}) 100,000 \text{ Hz} = \pi \times 10^6 \text{ V/s} = 3.14 \text{ V/\mu s}. \)
Problems 2.75

Sketch the output voltage of the circuit shown below to scale against time. Sometimes an integrator circuit is used as an (approximate) pulse counter. Suppose that the output voltage is -10V. How many input pulses have been applied? (Assume that the pulses have an amplitude of 5V and a duration of 2 ms, as shown in the other figure.)

For this integrator, with \( R = 10,000 \Omega \), and \( C = 2.0 \times 10^{-6} \text{F} \), the output voltage is given by:

\[
V_o(t) = -\frac{1}{RC} \int_0^t V_p(t') \, dt' = -50 \int_0^t V_p(t') \, dt'.
\]

When \( V_p = 5 \text{ V} \), the integral is proportional to \( t \) (it's equal to 5 \( t \)).

Then \((-50) \times 5 \times \frac{2 \text{ ms}}{0} = -0.5 \text{ Volt} \) for each pulse.

In other words, at the end of each pulse, the integrator output has decreased by 0.50 Volt.

-10V = (-0.5V/pulse) \times \text{n pulses} \implies \text{n = 20 pulses}

- Here is a graph of how the output evolves: